CLAIM AMENDMENTS

Please amend claims 1, 3-5, 7-10, 20-21, 30-31, and 41-42 as follows.

1.   (Currently Amended) A method, comprising:

allocating a first memory bandwidth; [[and]]

increasing the first memory bandwidth to a second memory bandwidth if a demand for memory bandwidth is less than the first memory bandwidth; and

decreasing the first memory bandwidth to a third memory bandwidth if a demand for memory bandwidth is greater than the first memory bandwidth.

2.   (Previously Presented) The method of claim 1, further comprising:

setting a window of time to monitor the demand for memory bandwidth; and

measuring the demand for memory bandwidth during the window of time.

3.   (Currently Amended) The method of claim 1, further comprising applying a mask to increase the memory bandwidth [[to a]] if a demand for memory bandwidth is less than the first memory bandwidth.

4.   (Currently Amended) The method of claim 1, further comprising applying a mask to decrease the memory bandwidth to a value the third memory bandwidth lower than the first value if a demand for memory bandwidth [[an]] by the memory controller is less than the first value memory bandwidth.

5.   (Currently Amended) An article of manufacture article of manufacture, comprising:

a machine-accessible medium including data that, when accessed by a machine, cause the machine to perform the operations comprising,

allocating a first memory bandwidth; [[and]]

increasing the first memory bandwidth to a second memory bandwidth if a demand for memory bandwidth is less than the first memory bandwidth; and

decreasing the first memory bandwidth <u>to a third memory bandwidth</u> if a demand for memory bandwidth is greater than the first memory bandwidth.

6. (Previously Presented) The article of manufacture of claim 5, wherein the machine-accessible medium further includes data that cause the machine to perform operations comprising:

setting a window of time to monitor the demand for memory bandwidth; and

measuring the demand for memory bandwidth during the window of time.

7. (Currently Amended) The article of manufacture of claim 5, wherein the machine-accessible medium further includes data that cause the machine to perform operations comprising applying a mask to increase the memory bandwidth [[to a]] if a demand for memory bandwidth is less than the first memory <u>bandwidth</u>.

8. (Currently Amended) The article of manufacture of claim 5, wherein the machine-accessible medium further includes data that cause the machine to perform operations comprising applying a mask to decrease the memory <u>bandwidth</u> to ~~a value lower than the first value~~ if a demand for memory bandwidth by the memory controller is less than the first ~~value~~ <u>memory</u> bandwidth.

9. (Currently Amended) An apparatus, comprising:

a memory controller to increase a memory bandwidth <u>from a first memory bandwidth to a second memory bandwidth</u> if a demand for the memory bandwidth is less than [[a]] <u>the</u> first memory bandwidth, the memory controller to decrease the memory bandwidth <u>to a third memory bandwidth</u> if the demand for the memory bandwidth is greater than the first memory bandwidth.

10. (Currently Amended) The apparatus of claim 9, further comprising:

a first register in the memory controller to set the <u>first</u> memory bandwidth;

a second register in the memory controller to set a window of time to monitor demand for memory bandwidth; and

a counter in the memory controller to measure demand for memory bandwidth during the window of time.

11. (Previously Presented) The apparatus of claim 10, wherein the memory controller further comprises a mask to increase the memory bandwidth if demand for memory bandwidth is less than the first memory bandwidth.

12. (Previously Presented) The apparatus of claim 10, wherein the memory controller further comprises a mask to decrease the memory bandwidth if demand for memory bandwidth is greater than the first memory bandwidth.

13. (Previously Presented) The apparatus of claim 9, further comprising:
a graphics controller to increase a graphics memory bandwidth if a demand for the graphics memory bandwidth is less than a first graphics memory bandwidth, the graphics controller to decrease graphics memory bandwidth if the demand for the graphics memory bandwidth is greater than the first graphics memory bandwidth.

14. (Previously Presented) The apparatus of claim 13, further comprising one or more input/output (I/O) devices, an individual I/O device having a second graphics memory bandwidth, the graphics controller to increase the graphics memory bandwidth if a demand for the graphics memory bandwidth by the I/O device is less than the second graphics memory bandwidth, the graphics controller to decrease the graphics memory bandwidth if a demand for the graphics memory bandwidth by the I/O device is greater than the second graphics memory bandwidth.

15. (Previously Presented) The apparatus of claim 13, further comprising a processor having a second graphics memory bandwidth, the graphics controller to increase the graphics memory bandwidth if a demand for the graphics memory bandwidth by the processor is less than the second graphics memory bandwidth, the graphics controller to decrease the percentage of graphics memory bandwidth if a demand for the graphics memory bandwidth by the processor is more than the second graphics memory bandwidth.

16.   (Previously Presented) The apparatus of claim 9, further comprising a graphics memory having a first graphics memory bandwidth, the graphics memory to increase graphics memory bandwidth if a demand for graphics memory bandwidth is less than the first graphics memory bandwidth, the graphics memory to decrease the graphics memory bandwidth if a demand for graphics memory bandwidth is greater than the first graphics memory bandwidth.

17.   (Previously Presented) The apparatus of claim 16, further comprising one or more input/output (I/O) devices, an individual I/O device having the first graphics memory bandwidth, the graphics memory to increase graphics memory bandwidth if a demand for the graphics memory bandwidth by the I/O device is less than the first graphics memory bandwidth, the graphics memory to decrease the graphics memory bandwidth if a demand for the graphics memory bandwidth by the I/O device is greater than the first graphics memory bandwidth.

18.   (Previously Presented) The apparatus of claim 16, further comprising a processor having a second graphics memory bandwidth, the graphics memory to increase the graphics memory bandwidth if a demand for graphics memory bandwidth by the processor is less than the second graphics memory bandwidth, the graphics memory to decrease the graphics memory bandwidth if a demand for graphics memory bandwidth by the processor is greater than the second graphics memory bandwidth.

19.   (Previously Presented) The apparatus of claim 9, further comprising one or more input/output (I/O) devices having a first memory bandwidth, wherein the memory controller is to increase the memory bandwidth if a demand for the memory bandwidth by the one or more I/O devices is less than the first memory bandwidth, the memory controller to decrease the memory bandwidth if a demand for the memory bandwidth by the one or more I/O devices is greater than the first memory bandwidth.

20.   (Currently Amended) An apparatus, comprising:

a processor having a first memory bandwidth, the processor having further a memory controller to increase the first memory bandwidth to a second memory bandwidth if a demand for the memory bandwidth by the processor is less than the first memory bandwidth, the memory

controller to decrease the first memory bandwidth <u>to a third memory bandwidth</u> if a demand for memory bandwidth by the processor is greater than the first memory bandwidth.

21.   (Currently Amended) The apparatus of claim 20, further comprising:
        a first register in the memory controller to set the <u>first</u> memory bandwidth;
        a second register in the memory controller to set a window of time to monitor demand for memory bandwidth; and
        a counter in the memory controller to measure demand for memory bandwidth during the window of time.

22.   (Previously Presented) The apparatus of claim 20, wherein the memory controller further comprises a mask to increase the memory bandwidth if demand for memory bandwidth is less than the first memory bandwidth.

23.   (Previously Presented) The apparatus of claim 20, wherein the memory controller further comprises a mask to decrease the memory bandwidth if demand for memory bandwidth is greater than the first memory bandwidth.

24-29. (Canceled)

30.   (Currently Amended) A system, comprising:
        a direct random access memory; and
        a memory controller to increase a memory bandwidth <u>from a first memory bandwidth to a second memory bandwidth</u> if a demand for the memory bandwidth is less than [[a]] <u>the</u> first memory bandwidth, the memory controller to decrease the memory bandwidth <u>from the first memory bandwidth to a third memory bandwidth</u> if the demand for the memory bandwidth is greater than the first memory bandwidth.

31.   (Currently Amended) The system of claim 30, further comprising:
        a first register in the memory controller to set the <u>first</u> memory bandwidth;
        a second register in the memory controller to set a window of time to monitor demand for

memory bandwidth; and

       a counter in the memory controller to measure demand for memory bandwidth during the window of time.

32.   (Previously Presented) The apparatus of claim 31, wherein the memory controller further comprises a mask to increase the memory bandwidth if demand for memory bandwidth is less than the first memory bandwidth.

33.   (Previously Presented) The system of claim 31, wherein the memory controller further comprises a mask to decrease the memory bandwidth if demand for memory bandwidth is greater than the first memory bandwidth.

34.   (Previously Presented) The system of claim 30, further comprising:

       a graphics controller to increase a graphics memory bandwidth if a demand for the graphics memory bandwidth is less than a first graphics memory bandwidth, the graphics controller to decrease graphics memory bandwidth if the demand for the graphics memory bandwidth is greater than the first graphics memory bandwidth.

35.   (Previously Presented) The system of claim 34, further comprising one or more input/output (I/O) devices, an individual I/O device having a second graphics memory bandwidth, the graphics controller to increase the graphics memory bandwidth if a demand for the graphics memory bandwidth by the I/O device is less than the second graphics memory bandwidth, the graphics controller to decrease the graphics memory bandwidth if a demand for the graphics memory bandwidth by the I/O device is greater than the second graphics memory bandwidth.

36.   (Previously Presented) The system of claim 34, further comprising a processor having a second graphics memory bandwidth, the graphics controller to increase the graphics memory bandwidth if a demand for the graphics memory bandwidth by the processor is less than the second graphics memory bandwidth, the graphics controller to decrease the percentage of

graphics memory bandwidth if a demand for the graphics memory bandwidth by the processor is more than the second graphics memory bandwidth.

37.   (Previously Presented) The system of claim 30, further comprising a graphics memory having a first graphics memory bandwidth, the graphics memory to increase graphics memory bandwidth if a demand for graphics memory bandwidth is less than the first graphics memory bandwidth, the graphics memory to decrease the graphics memory bandwidth if a demand for graphics memory bandwidth is greater than the first graphics memory bandwidth.

38.   (Previously Presented) The system of claim 37, further comprising one or more input/output (I/O) devices, an individual I/O device having the first graphics memory bandwidth, the graphics memory to increase graphics memory bandwidth if a demand for the graphics memory bandwidth by the I/O device is less than the first graphics memory bandwidth, the graphics memory to decrease the graphics memory bandwidth if a demand for the graphics memory bandwidth by the I/O device is greater than the first graphics memory bandwidth.

39.   (Previously Presented) The system of claim 37, further comprising a processor having a second graphics memory bandwidth, the graphics memory to increase the graphics memory bandwidth if a demand for graphics memory bandwidth by the processor is less than the second graphics memory bandwidth, the graphics memory to decrease the graphics memory bandwidth if a demand for graphics memory bandwidth by the processor is greater than the second graphics memory bandwidth.

40.   (Previously Presented) The system of claim 30, further comprising one or more input/output (I/O) devices having a first memory bandwidth, wherein the memory controller is to increase the memory bandwidth if a demand for the memory bandwidth by the one or more I/O devices is less than the first memory bandwidth, the memory controller to decrease the memory bandwidth if a demand for the memory bandwidth by the one or more I/O devices is greater than the first memory bandwidth.

41.   (Currently Amended) A system, comprising:

a direct random access memory; and

a processor having a first memory bandwidth, the processor having further a memory controller to increase the first memory bandwidth from the first memory bandwidth to a second memory bandwidth if a demand for the memory bandwidth by the processor is less than the first memory bandwidth, the memory controller to decrease the first memory bandwidth from the first memory bandwidth to a third memory bandwidth if a demand for memory bandwidth by the processor is greater than the first memory bandwidth.

42.   (Currently Amended) The system of claim 41, further comprising:

a first register in the memory controller to set the first memory bandwidth;

a second register in the memory controller to set a window of time to monitor demand for memory bandwidth; and

a counter in the memory controller to measure demand for memory bandwidth during the window of time.

43.   (Previously Presented) The system of claim 41, wherein the memory controller further comprises a mask to increase the memory bandwidth if demand for memory bandwidth is less than the first memory bandwidth.

44.   (Previously Presented) The system of claim 41, wherein the memory controller further comprises a mask to decrease the memory bandwidth if demand for memory bandwidth is greater than the first memory bandwidth.